Quick Start Guide

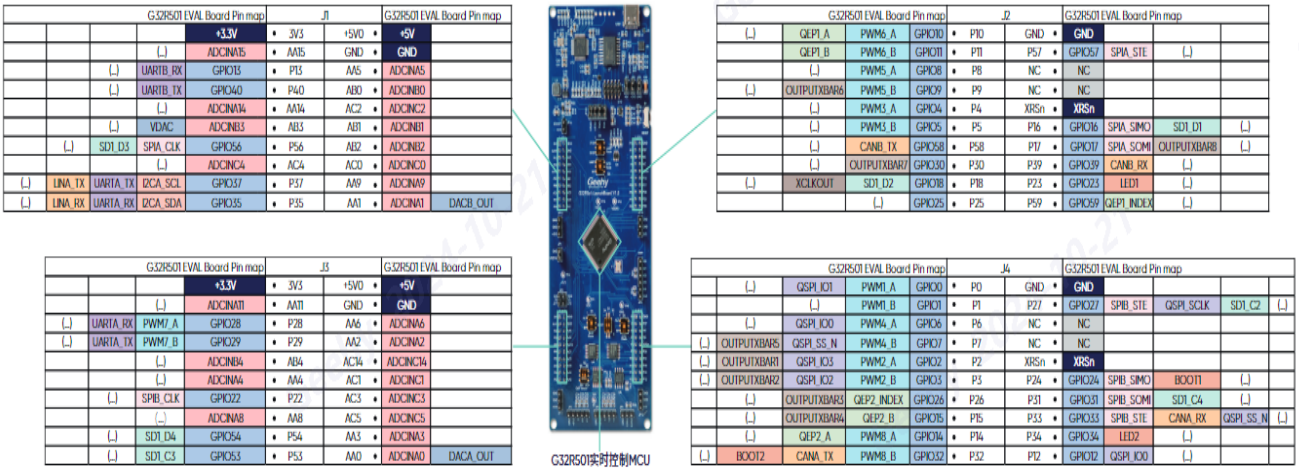
G32R501

Version: V1.0

Contents

1 PCB Function Introduction

Figure 1 G32R501 Evaluation Board Development Tool



Some characteristics of G32R501 Evaluation Board are worth noting, and they have been marked in the figure:

- USB isolation interface with power supply (USB1)
- USB isolation power jumper cap (JP7~JP9)
- Onboard Geehy-Link debugger (U12)
- JTAG/UART isolation jumper cap (JP16)
- Onboard LED (LED1, LED2)
- Reset button (B1)
- 40-pin ExpandPack Connector Site 1 (J1~J2)
- VREFHI jumper cap (JP1)
- G32R501 MCU (U1)
- 20MHz passive crystal oscillator (Y1)
- QSPI interface (JP6)
- 40-pin ExpandPack Connector Site 2 (J3~J4)
- Dial switch (S1~S6)
- EQEP1 and EQEP2 interfaces (JP3~JP4)
- CAN interface (JP5)

In this chapter, only the characteristics that need to be used are briefly explained. For more information about the G32R501 Evaluation Board development board, please refer to *G32R501 Evaluation Board User Guide*.

1.1 Boot Mode Selection Switch (S1)

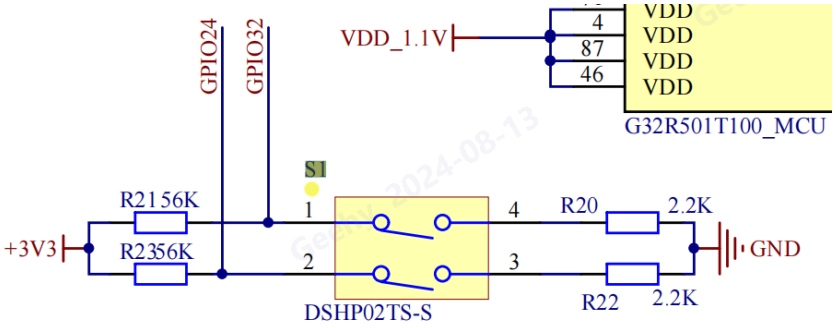
The Boot ROM of G32R501 contains the Bootloader program, which will be executed every time the device is powered on or reset. The two pins, GPIO24 and GPIO32, are connected to the Boot mode selection switch (S1). Please pay attention to the silk screen information on the PCB. The OFF (open) position of the switch corresponds to logic 1 (pin at high level), and the ON (closed) position of

the switch corresponds to logic 0 (pin at low level). By default, these two pins are set to the OFF position, so the device will boot from Flash. In addition to the four Boot modes listed in the table below, G32R501 also supports SPI, I2C, and many other flexible Bootloader configuration options. For more information about the boot mode, please refer to *G32R501 User Manual*.

Table 1 Boot Mode Selection Switch Settings

Boot mode	Gear 24 of S1	Gear 32 of S1
Flash (default)	1	1
UART / Wait Boot	0	1
CAN	1	0

Figure 2 Schematic Diagram of Boot Mode Selection Switch



1.2 Virtual COM Port Selection Switch (S4, S6)

G32R501 Evaluation Board allows one of the two groups of UARTA pins (GPIO37/35 and GPIO29/28) to be routed to the Geehy-Link virtual COM port. By default, GPIO28 (configurable as UARTA_RX) and GPIO29 (configurable as UARTA_TX) are routed to the virtual COM port, and are not available on the ExpandPack connector. Alternatively, GPIO35 (configurable as UARTA_RX) and GPIO37 (configurable as UARTA_TX) can be routed to the virtual COM port. When UART function is not required on the virtual COM port, GPIO can be routed to the ExpandPack connector to implement ExpandPack standard functions.

Table 2 Virtual COM Port Selection Switch Settings

UART mode	S4 gear	S6 gear
The GPIO29/28 of MCU is mapped to the Geehy-Link virtual COM port. The GPO29/28 pins on ExpandPack are unavailable. (Default)	UART	29/28
The GPIO37/35 of MCU is mapped to the Geehy-Link virtual COM port. The GPO37/35 pins on ExpandPack are unavailable.	UART	37/35
The GPIO37/35 and GPIO29/28 of MCU are mapped to the corresponding GPIO on the ExpandPack normally.	BP	Arbitrarily

1.3 Debugging and Interface (JP17)

The G32R501 Evaluation Board is equipped with a Geehy-Link hardware debugger. Users can use Geehy-Link for burning and debugging in Arm Keil MDK of version V5.40 and above. The Geehy-Link on the board is designed to support the 2pin JTAG mode, which means that it only uses the JTAG

pins of TMS and TCK, and allows reassignment of TDI and TDO according to application requirements.

Connector JP17 is used to debug external MCU using the onboard Geehy-Link hardware debugger. Through this connector, the Evaluation Board can be used as an independent Geehy-Link hardware debugger. If the Evaluation Board is used in this way, please ensure that all jumper caps of JP16 have been removed so as to isolate the JTAG signal and prevent it from entering the G32R501 MCU. Use an external debugger.

Table 3 Multiplex Function Switch Settings

Pin group	S1	S2	S3	S4	S5	S6	Function
GPIO28/GPIO29	x	x	x	0	x	0	UART is mapped to virtual COM port (default configuration)
	x	x	x	1	x	x	GPIO is mapped to ExpandPack Site2
GPIO35/GPIO37	x	x	1	x	x	1	GPIO is connected to EQEP port
	x	x	0	x	x	x	GPIO is mapped to ExpandPack Site2 (default configuration)
GPIO35/GPIO37/ GPIO59	x	0	x	x	x	x	QEP1 is mapped to GND
	x	1	x	x	x	x	GPIO is mapped to 3.3V (default configuration)
GPIO14/GPIO15/ GPIO26	x	0	x	x	x	x	QEP2 is mapped to GND
	x	1	x	x	x	x	GPIO is mapped to 3.3V (default configuration)
GPIO2/GPIO3	x	x	x	x	1	x	CAN is mapped to U6
	x	x	x	x	0	x	GPIO is mapped to ExpandPack Site2 (default configuration)

Note: "x" represents that the status of the switch has no impact on specific functions.

2 Environment Setup

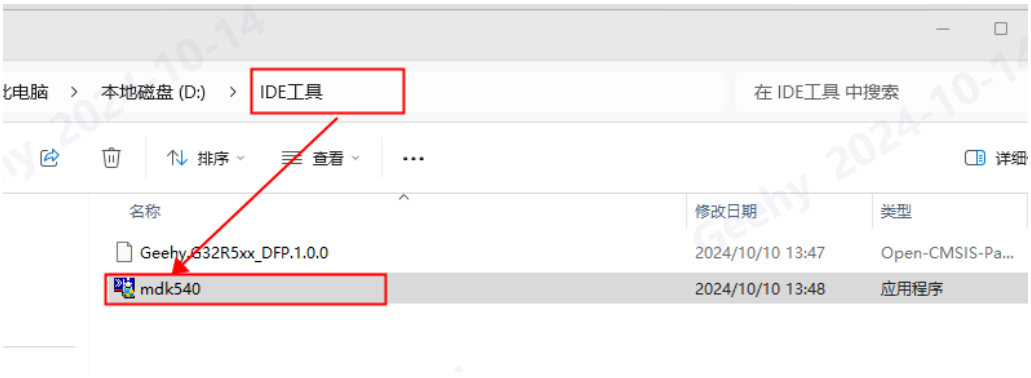
2.1 Introduction

The core of G32R501 is Cortex-M52, based on Arm v8.1-M architecture, which has a series of new features compared to other architectures, and has certain requirements for tool chains. Before developing G32R501, it is necessary to set up an IDE integrated development environment.

(1) Tool preparation

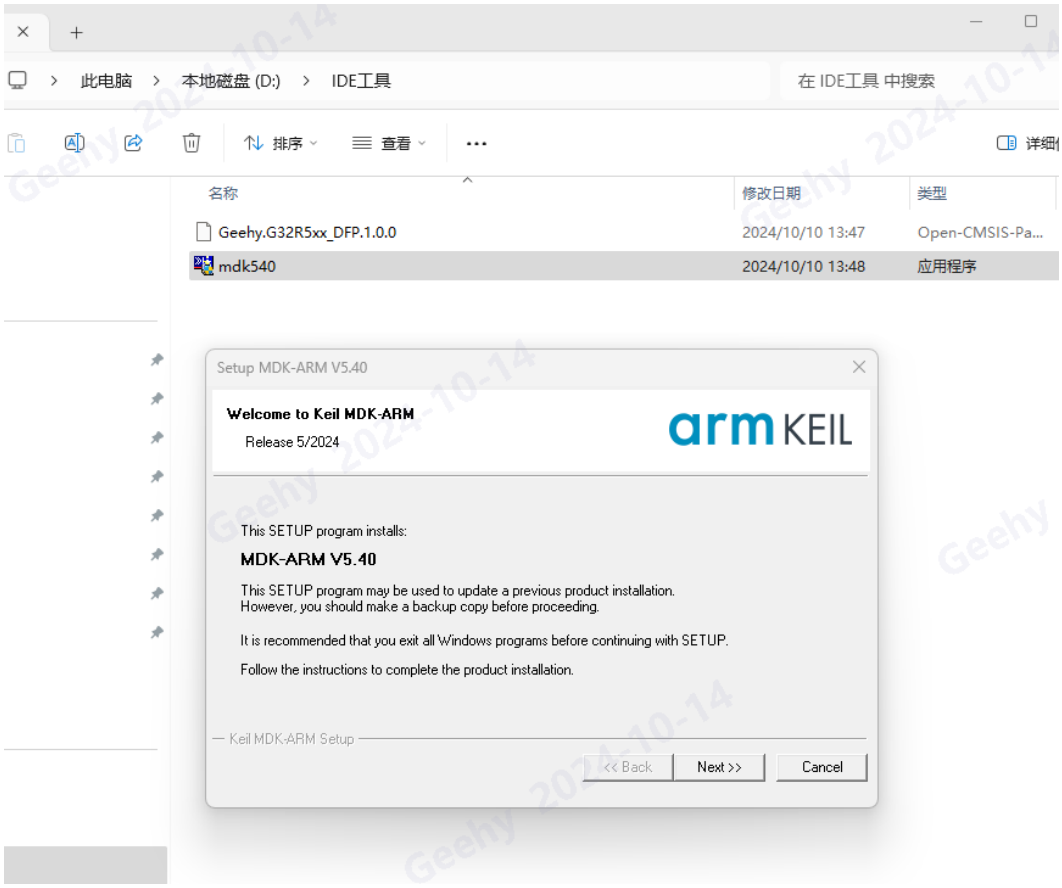
IDE tool: MDK-Arm Version 5.41 with official authorization.

DE address: Arm Keil MDK official website: https://www.keil.arm.com/mdk-community/.

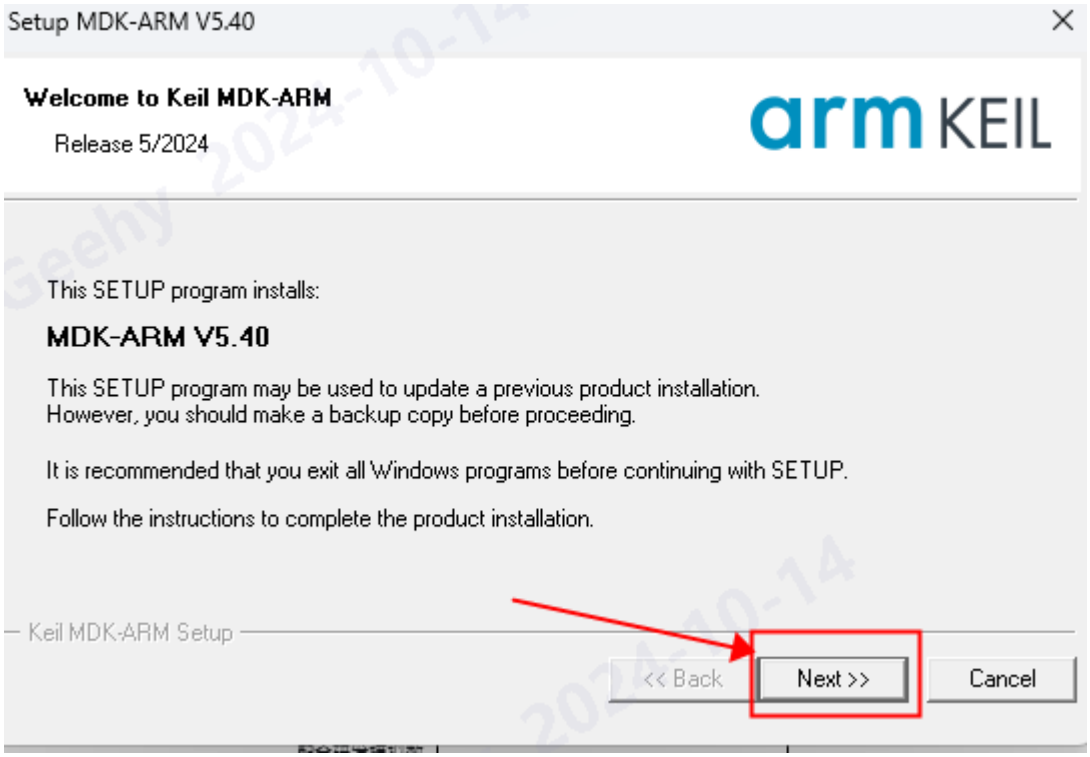


(2) IDE installation steps:

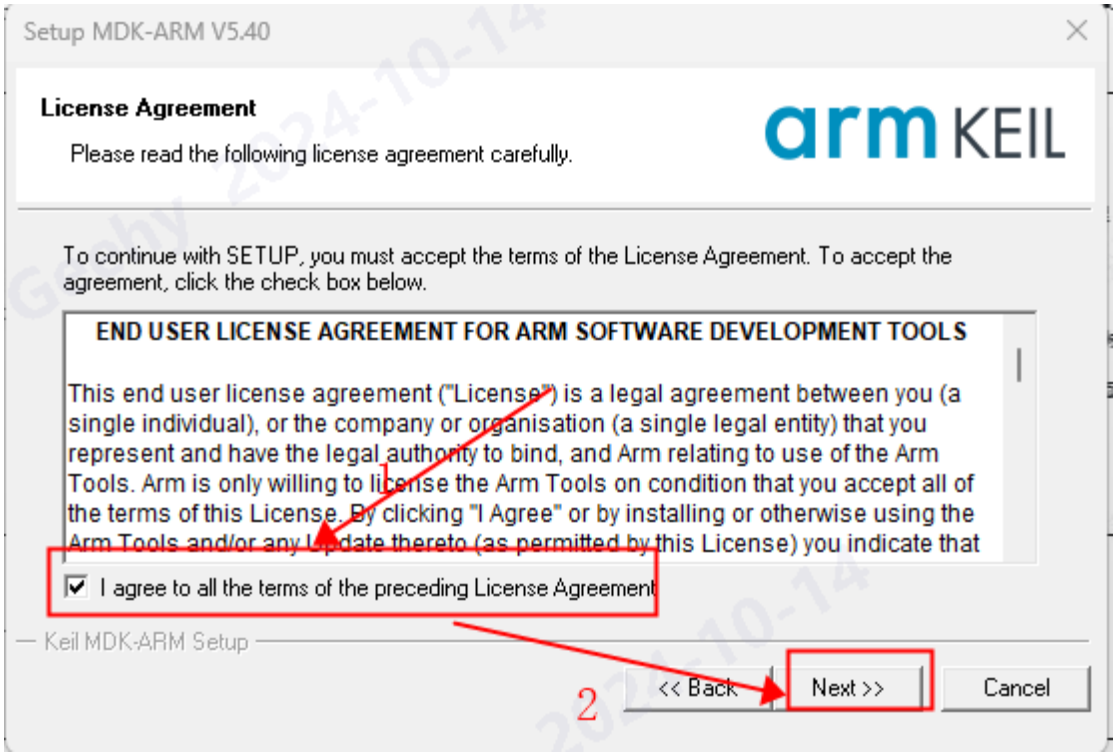
Double-click [mdk540] installation package to open MDK-Arm V5.40, as shown in the figure:

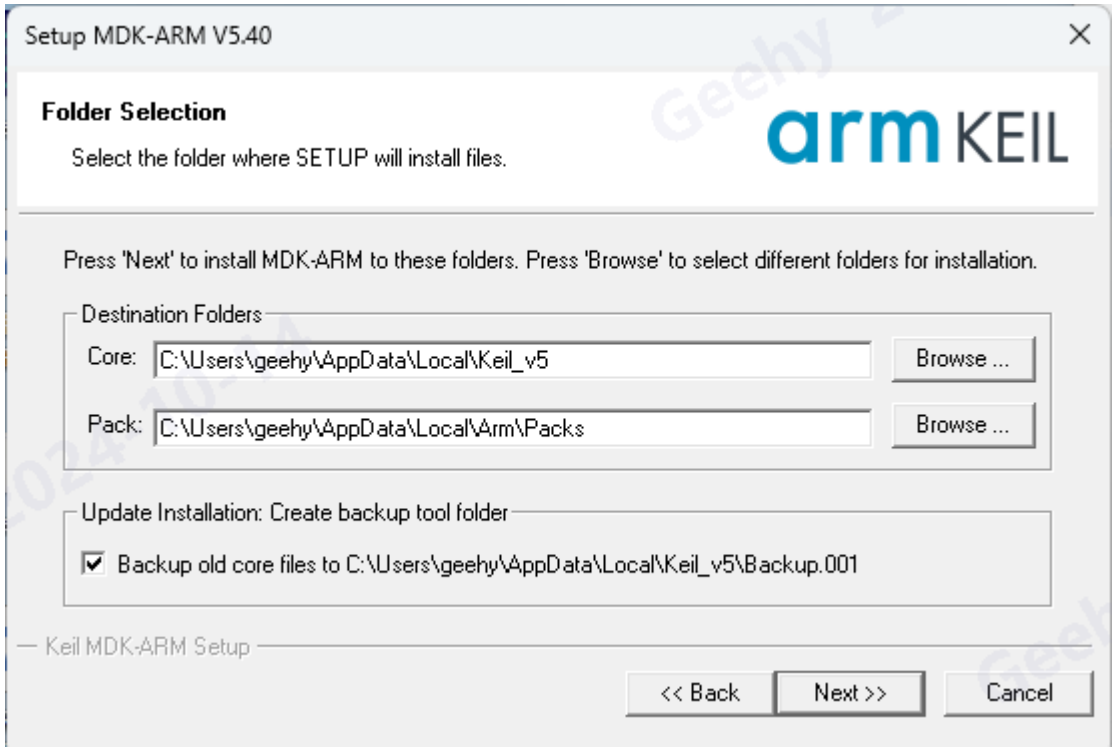


(3) Click [Next>>] to enter the interface shown in the figure below:

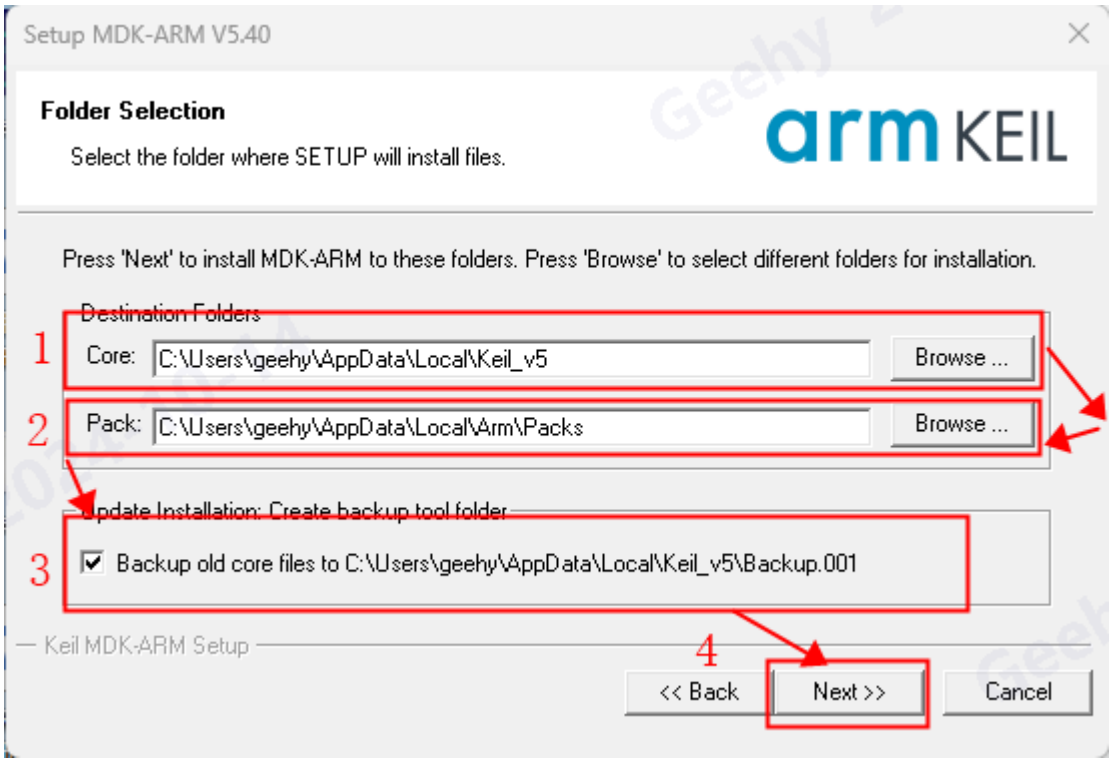


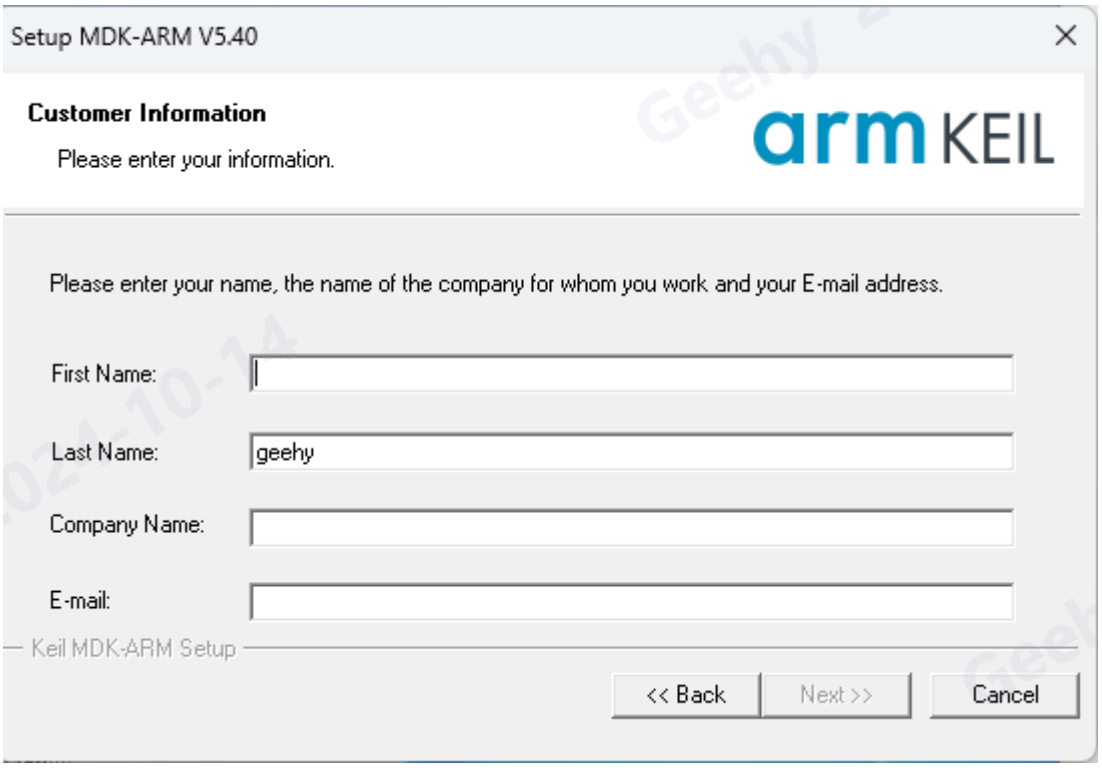
(4) Check [License Agreement] and click [Next>>] to enter the interface shown in the figure below:



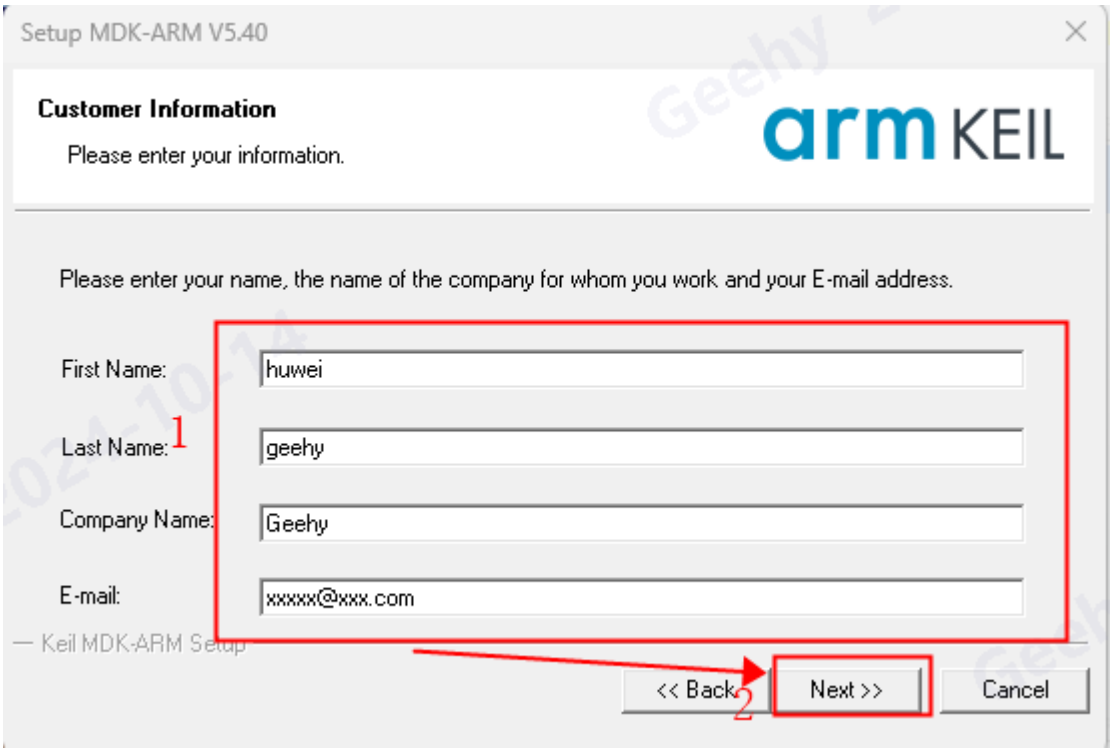


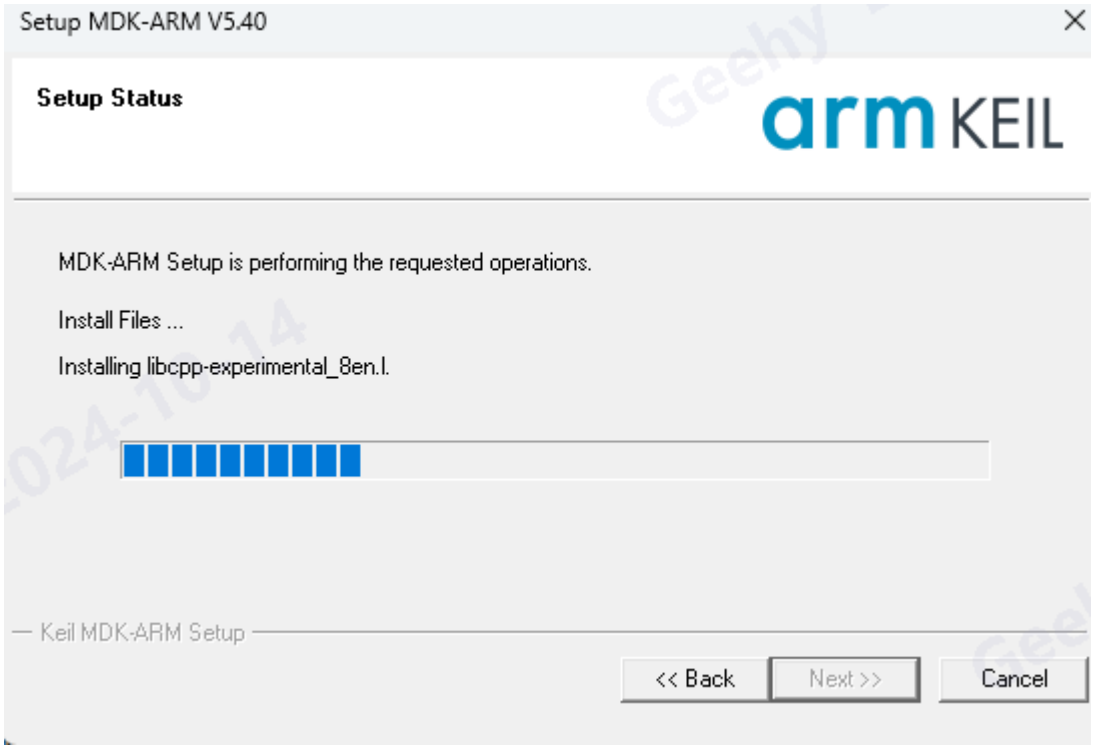
(5) Set the Keil_v5 tool and PACK package installation path (default installation path is recommended), check the [Update Installation] option and then click [Next>>] to enter the interface shown in the figure below:



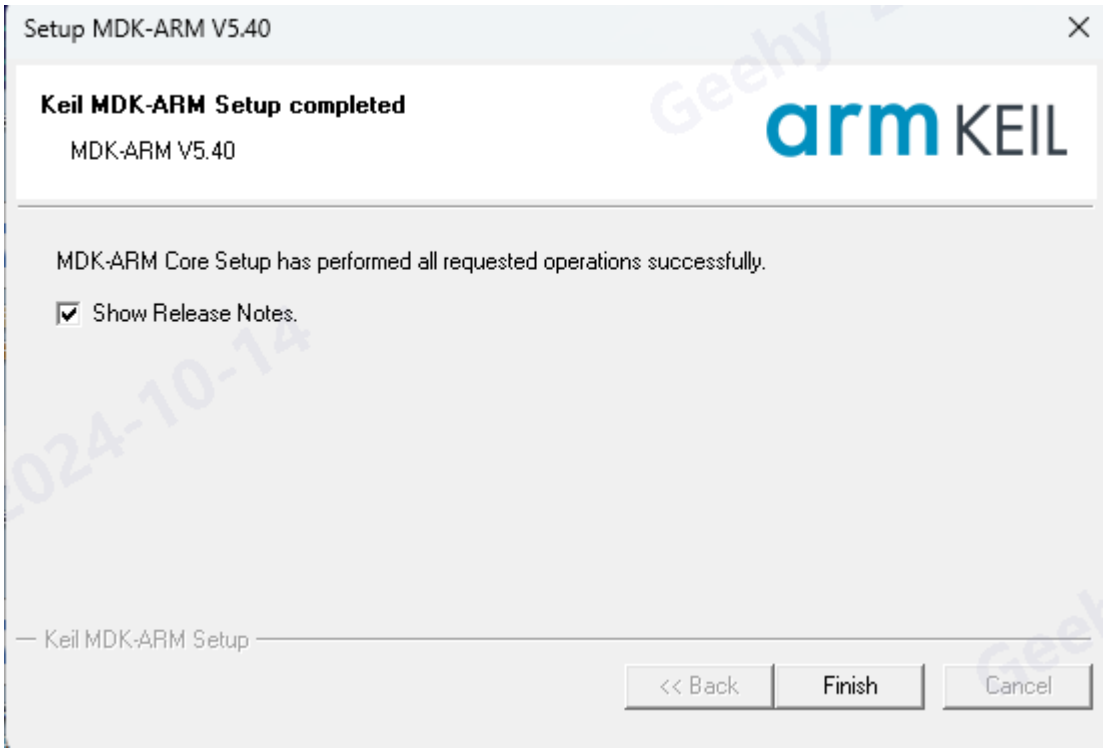


(6) Fill in [First Name], [Last Name], [Company Name] and [E-mail], and click [Next>>] to enter the interface shown in the figure below:





(7) After successful installation, click [finish]


Setup MDK-ARM V5.40
Keil MDK-ARM Setup completed
MDK-ARM V5.40
arm KEIL
MDK-ARM Core Setup has performed all requested operations successfully.
Show Release Notes.
Keil MDK-ARM Setup
<< Back
Finish
Cancel

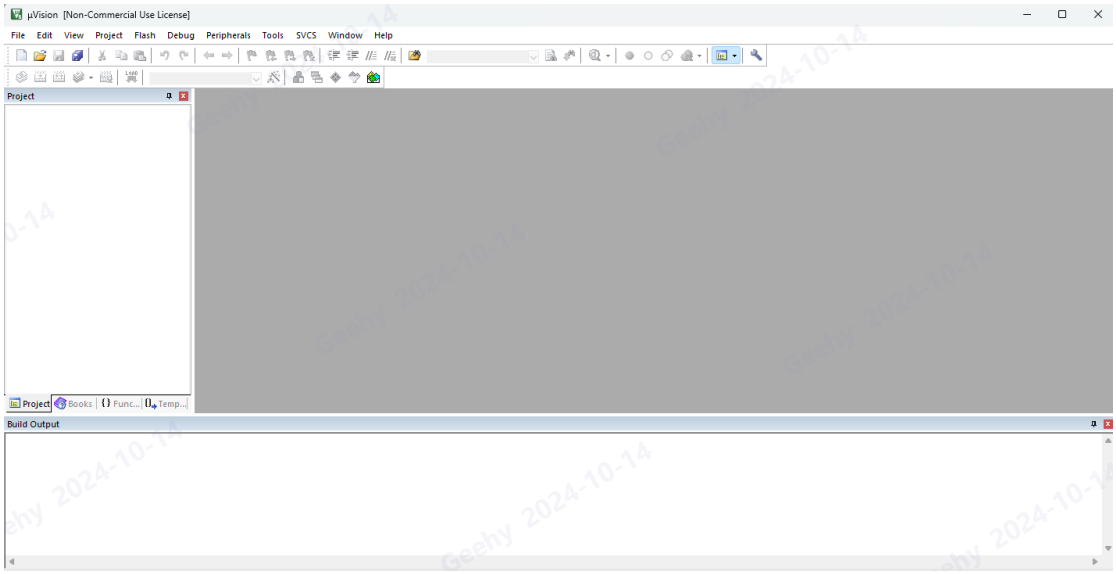
3 PACK Package Installation

Geehy.G32R5xx_DFP.1.0.0.pack is a software package provided by Geehy and used in Keil. It includes libraries, drivers, header files, sample codes, and corresponding documents used for G32R501.

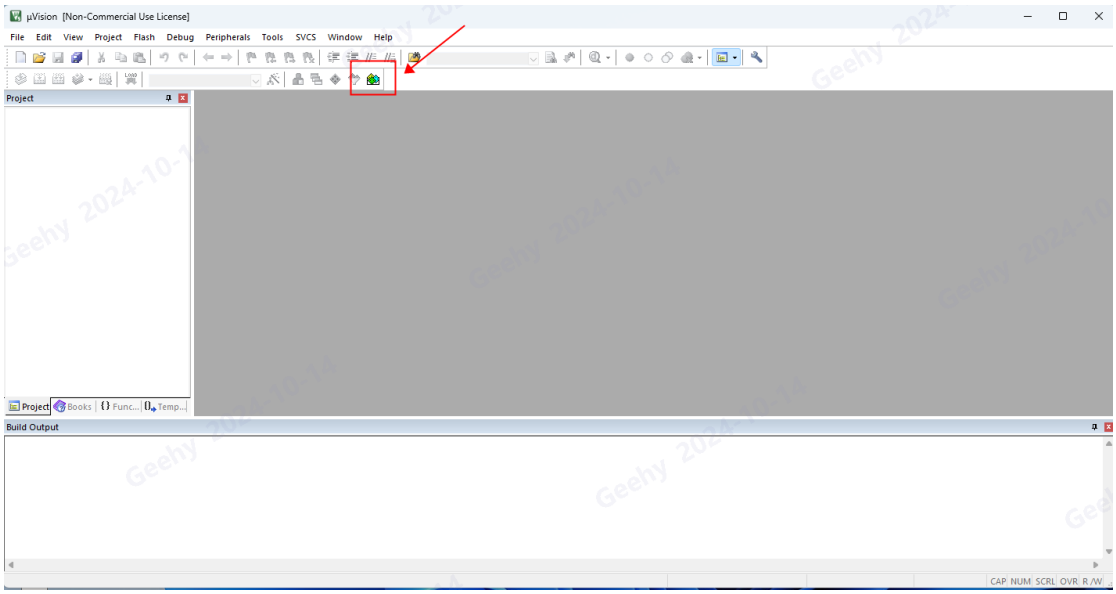
Please find the software package file in package folder of SDK folder, and it is located at:

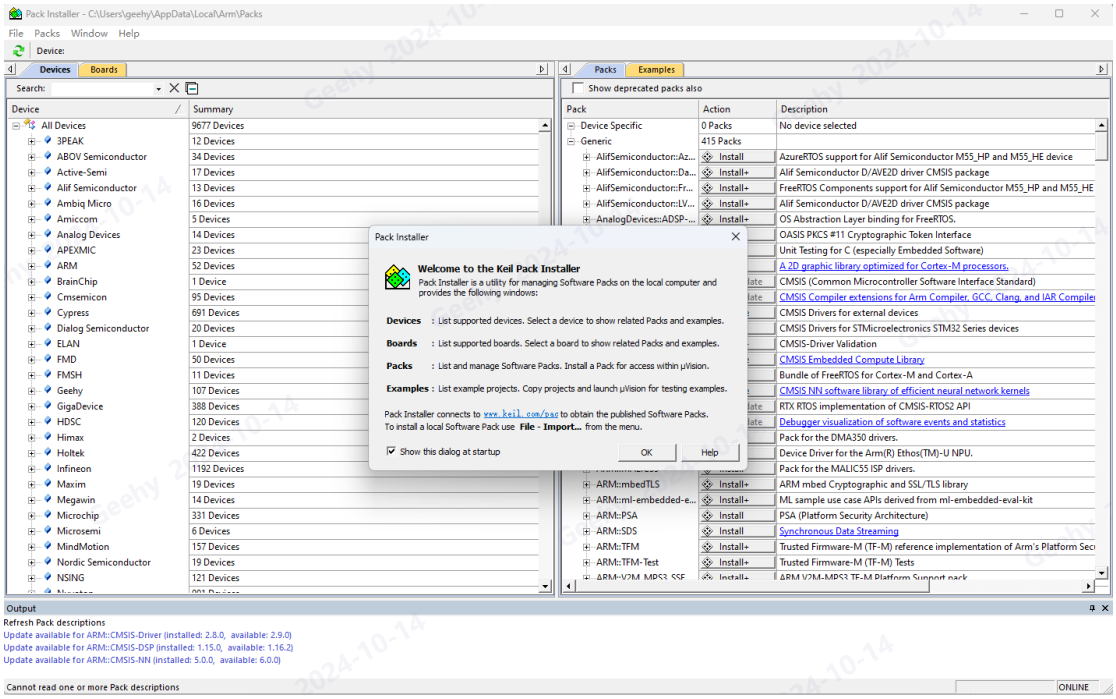
… / … / Geehy.G32R5xx_DFP.1.0.0.pack (the specific location is provided by FAE)

(1) Click Keil IDE to enter the interface shown in the figure below:

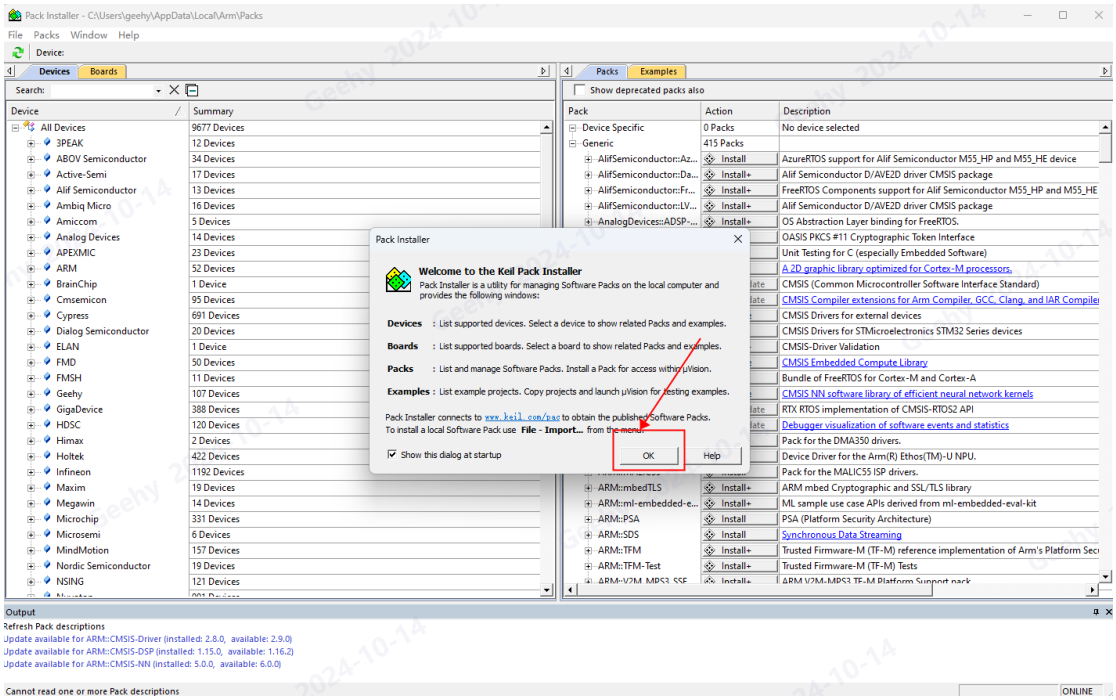


(2) Click to open [Pack Installer] and enter the interface shown in the figure below:

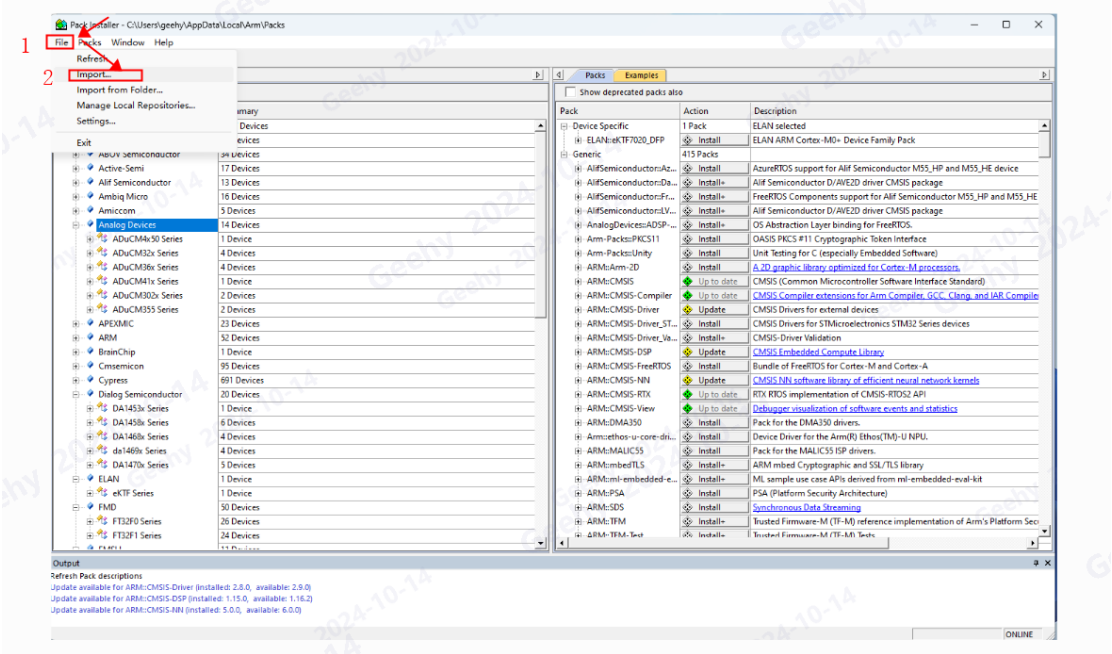




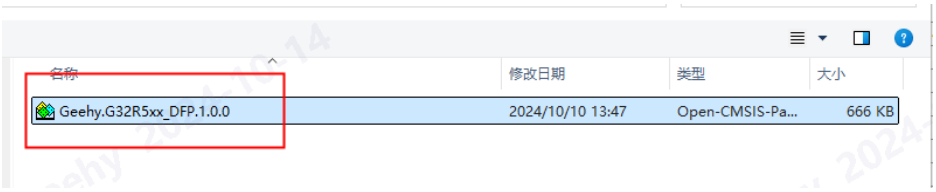
(3) Click [OK], as shown in the figure below:



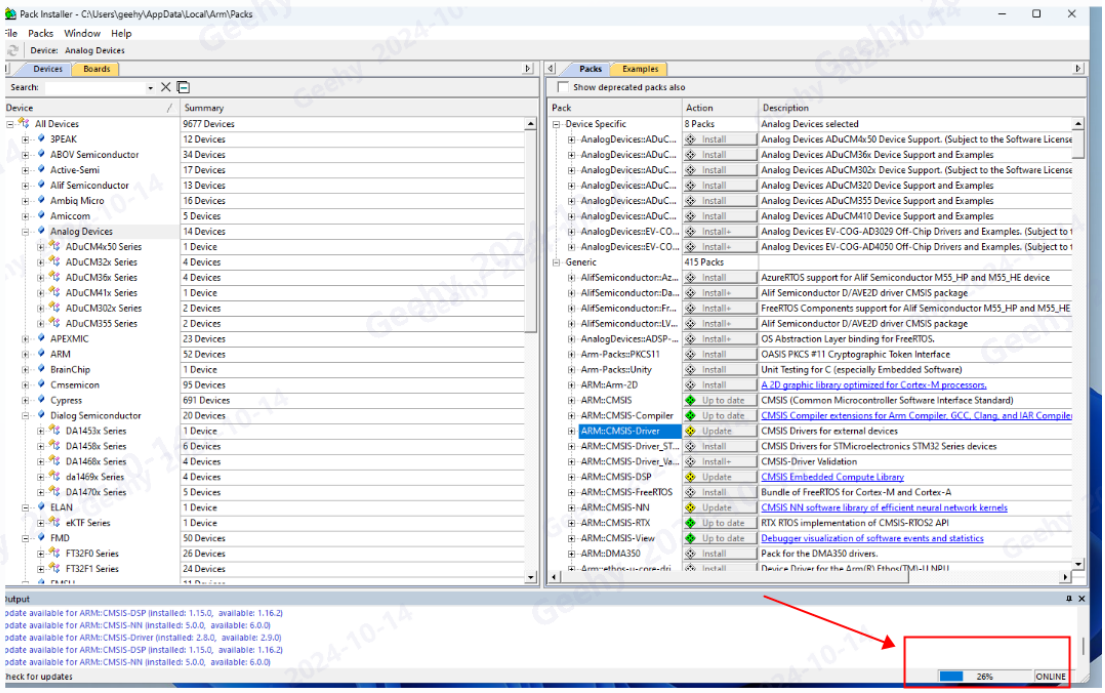
(4) Click [File] to display the drop-down menu, as shown in the interface below:



(5) Click [import] to enter the import Pcak interface and select Geehy.G32R5xx_DFP.1.0.0 file, as shown in the following figure:



(6) 7. When the progress bar reaches 100%, the pack installation is completed.



4 Engineering Configuration, Import, and Compilation

4.1 Import Project

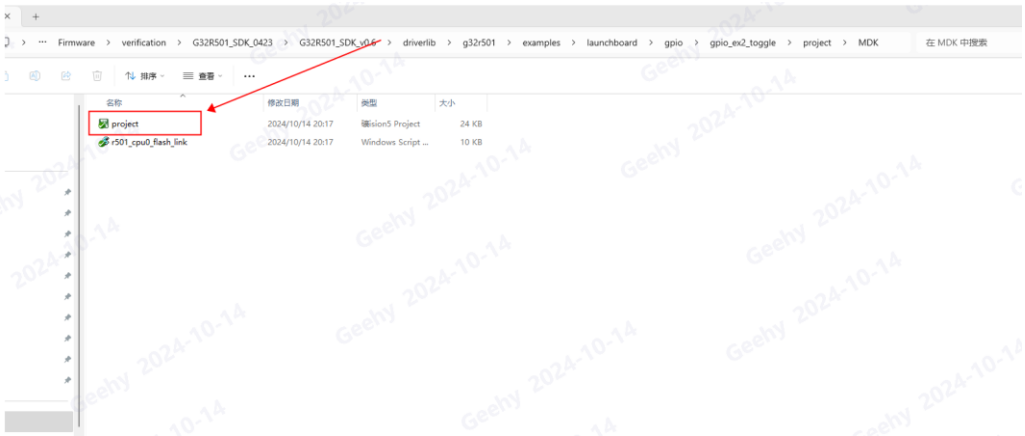
Example routine: gpio_ex2_toggle

Example relative path:

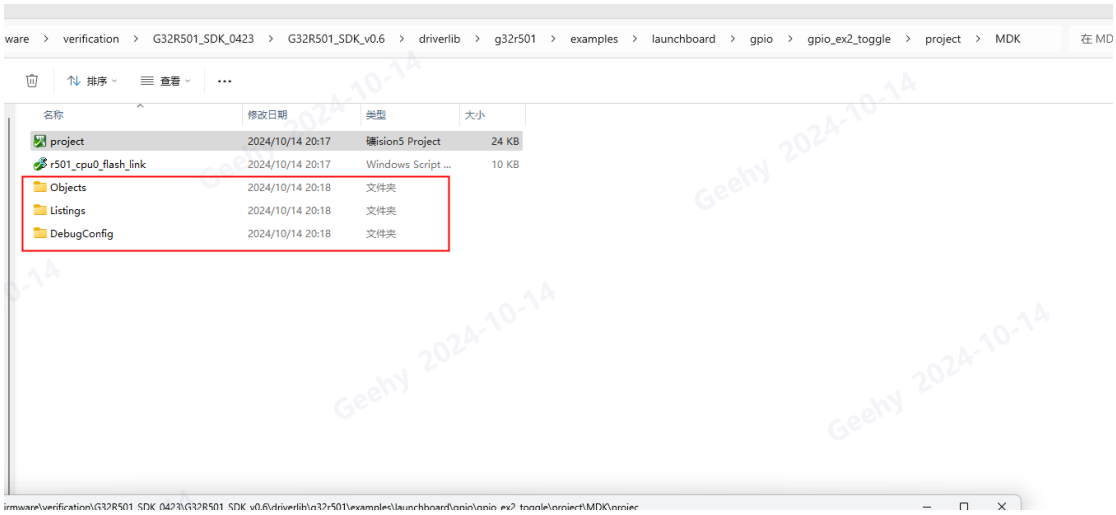
G32R501_SDK_v0.6\driverlib\g32r501\examples\launchboard\gpio\gpio_ex2_toggle

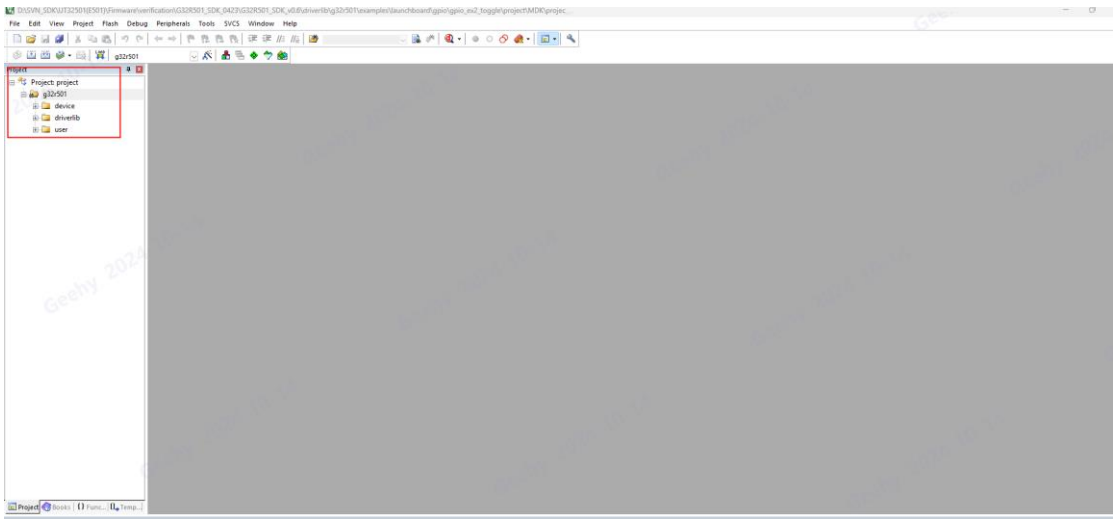
Import steps:

(1) Enter the folder gpio_ex2_toggle->project->MDK, find the file named project, as shown in the figure below:



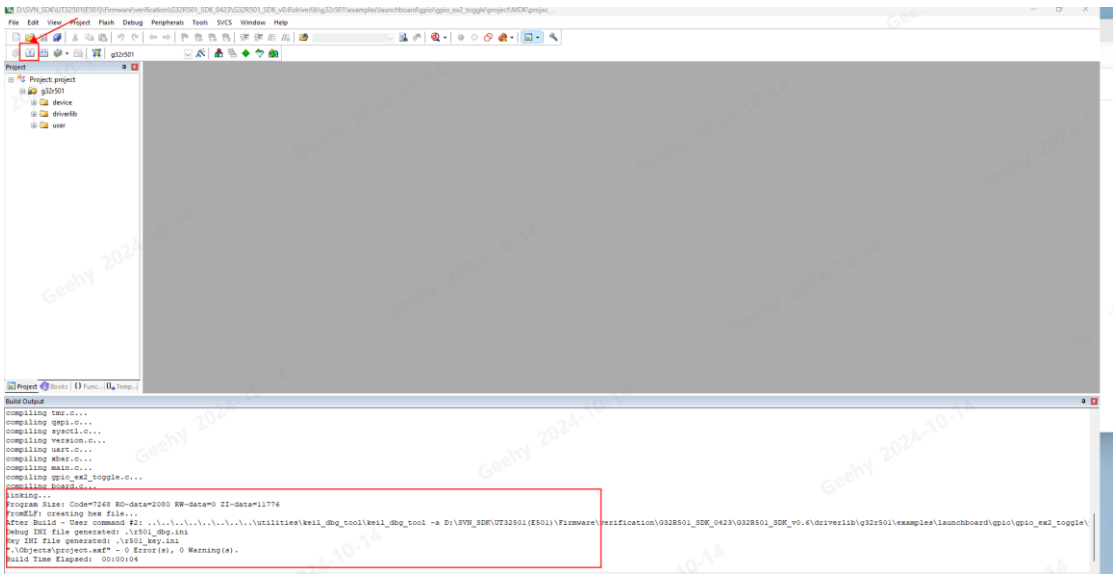
(2) Double-click the project file to open it, the Object, Listings, and Debug will be automatically generated, and the project will be displayed in Keil IDE, as shown in the figure below:



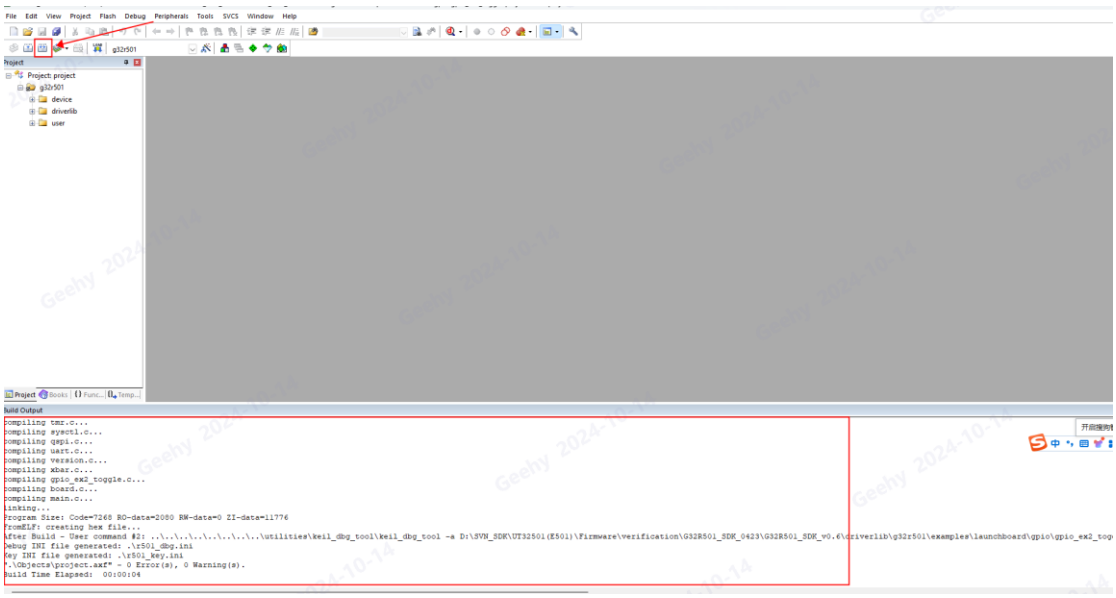


(3) Click the function bar Build to compile, and then view the errors in the Build Output information bar, as shown in the figure below:

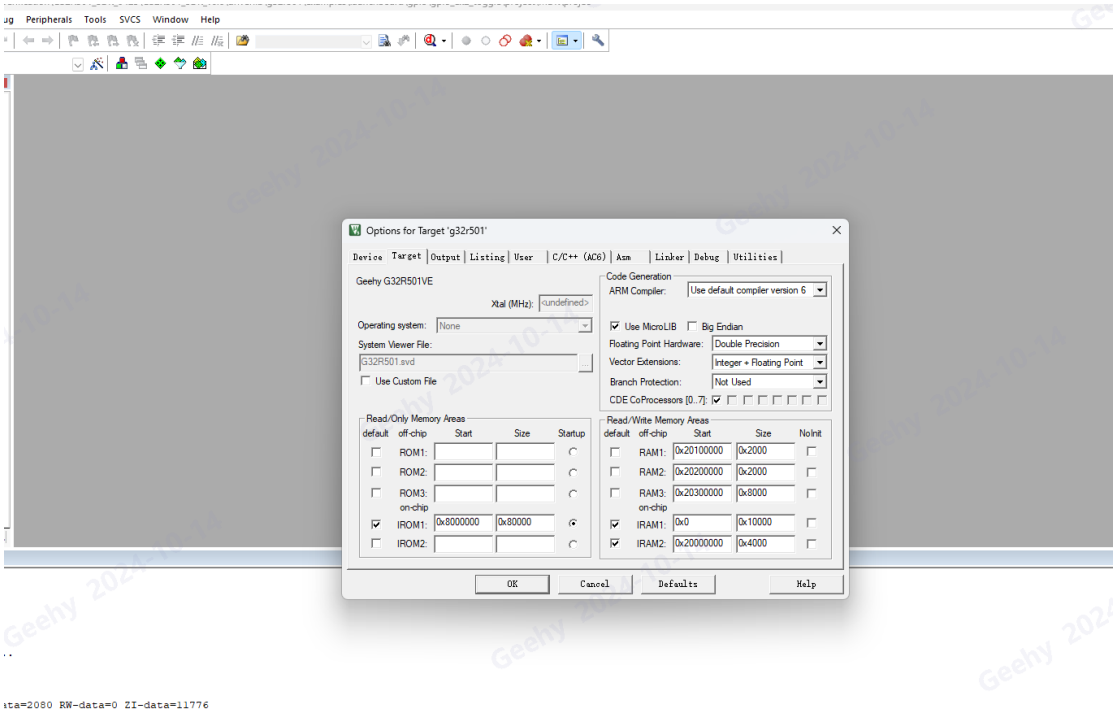
(Choose either Step 3 or Step 4)



(4) Click Rebuild to compile, and then view the errors in the Build Output information bar, as shown in the figure below: (Choose either Step 3 or Step 4)

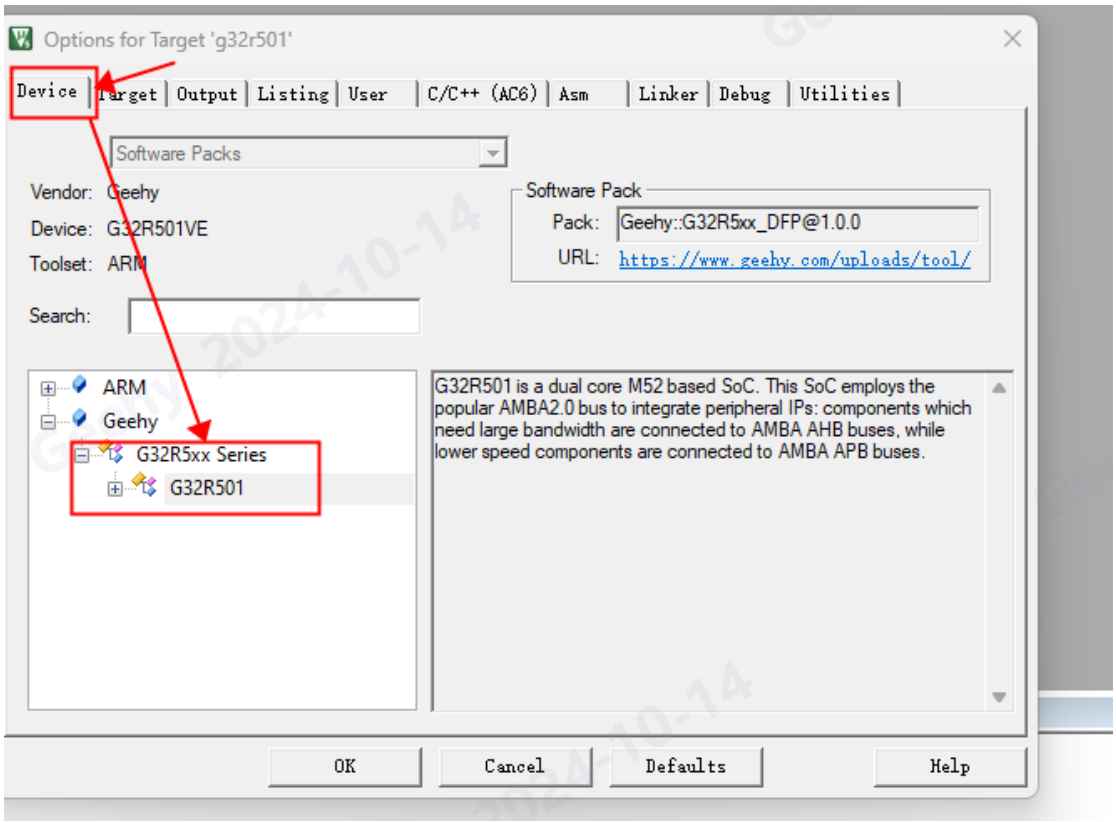


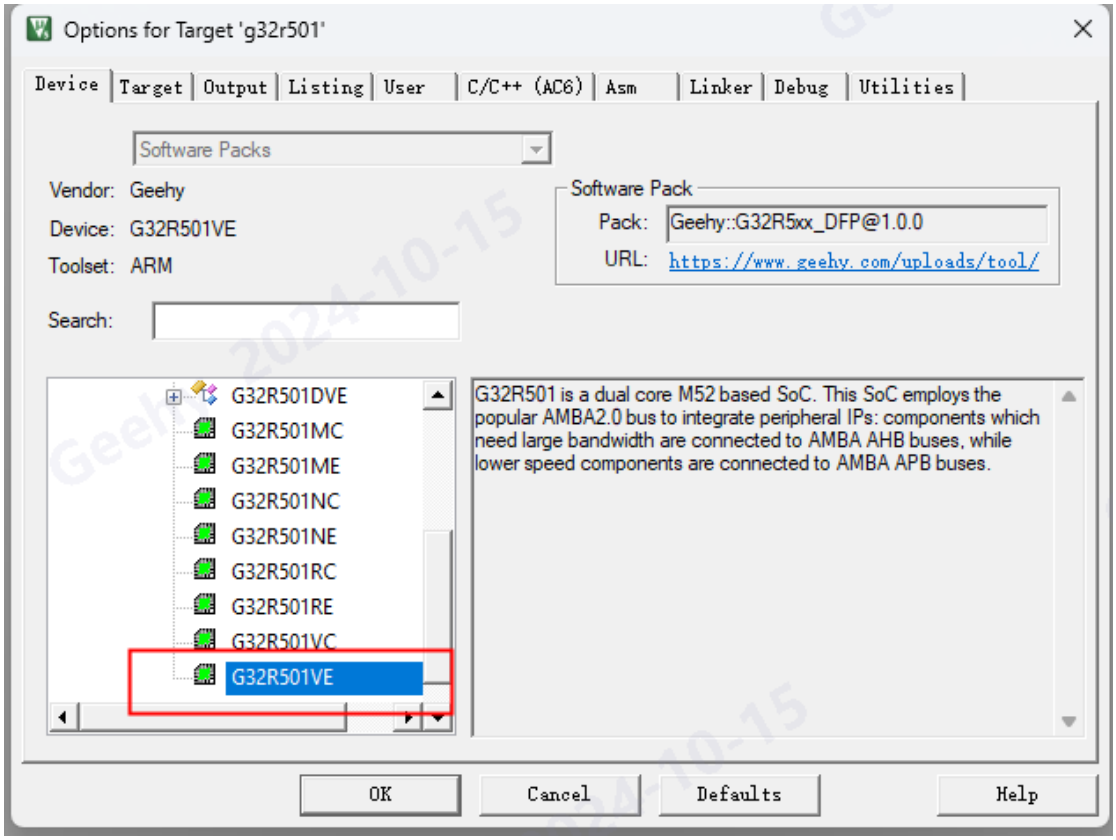
(5) Click Options for Target “Magic Wand” and the following interface will appear:



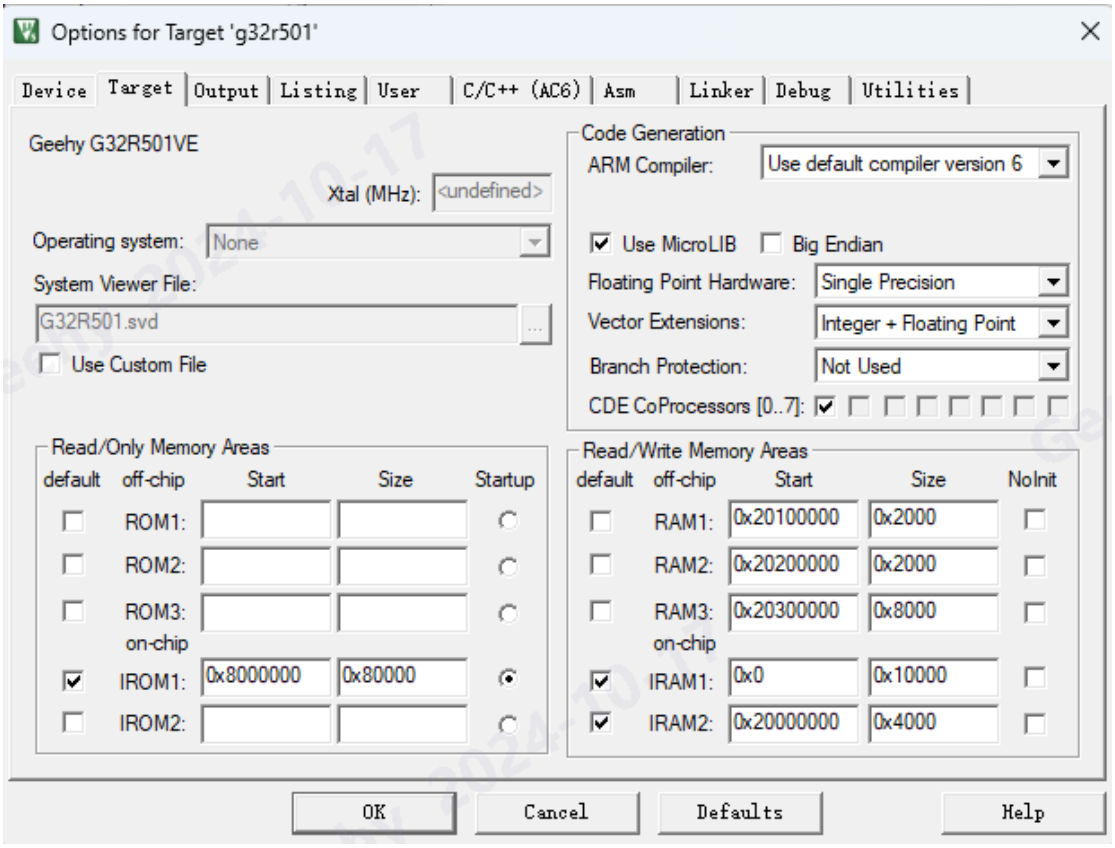
(6) Configure in the Option for Target interface, select the Device column, expand Geehy->G32R5xx Series

->G32R501->G32R501DVE, and select G32R501DVE:

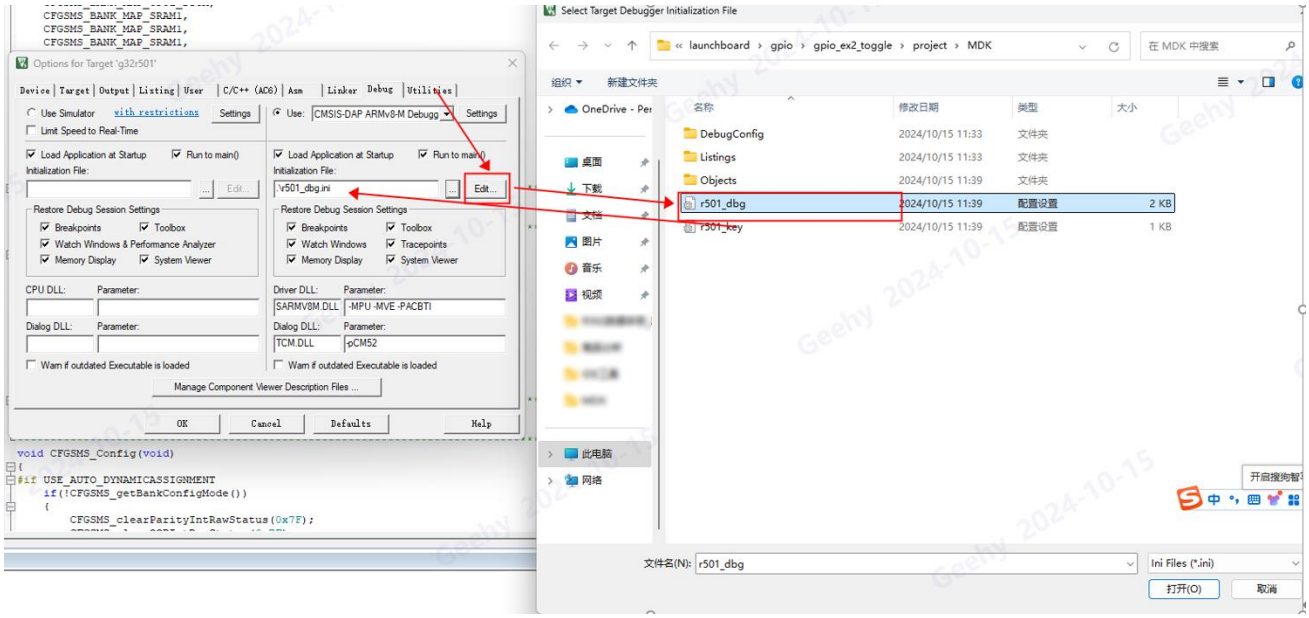

Options for Target 'g32r501'
Device
Target
Output
Listing
User
C/C++ (AC6)
Asm
Linker
Debug
Utilities
Software Packs
Vendor: Geehy
Device: G32R501VE
Toolset: ARM
Search:
Software Pack
Pack: Geehy::G32R5xx_DFP@1.0.0
URL: https://www.geehy.com/uploads/tool/
ARM
Geehy
G32R5xx Series
G32R501
G32R501 is a dual core M52 based SoC. This SoC employs the popular AMBA2.0 bus to integrate peripheral IPs: components which need large bandwidth are connected to AMBA AHB buses, while lower speed components are connected to AMBA APB buses.
OK
Cancel
Defaults
Help

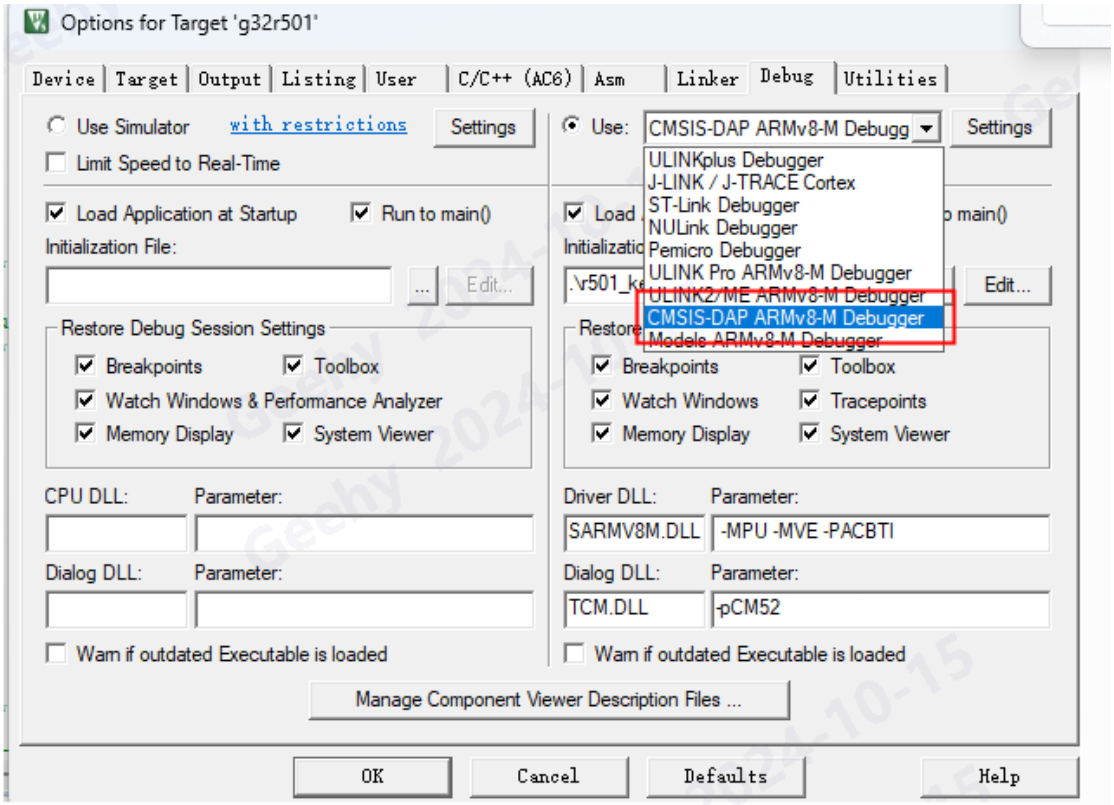

Options for Target 'g32r501'
Device
Target
Output
Listing
User
C/C++ (AC6)
Asm
Linker
Debug
Utilities
Software Packs
Vendor: Geehy
Device: G32R501VE
Toolset: ARM
Search:
Software Pack
Pack: Geehy::G32R5xx_DFP@1.0.0
URL: https://www.geehy.com/uploads/tool/
G32R501DVE
G32R501MC
G32R501ME
G32R501NC
G32R501NE
G32R501RC
G32R501RE
G32R501VC
G32R501VE
G32R501 is a dual core M52 based SoC. This SoC employs the popular AMBA2.0 bus to integrate peripheral IPs: components which need large bandwidth are connected to AMBA AHB buses, while lower speed components are connected to AMBA APB buses.
OK
Cancel
Defaults
Help

(7) Configure in the Option for Target interface, select the Target column, and check the configuration of IROM1, IRAM1, IRAM2, RAM1, and RAM2 addresses and sizes, as shown in the following figure:

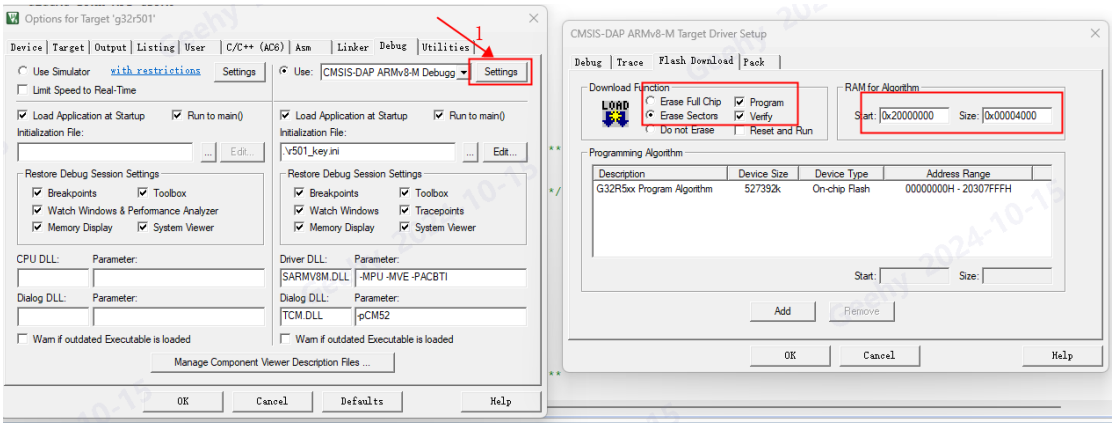


(8) Configure in the Option for Target interface, select the Debug column, choose CMSIS-DAP ARMv8-M Debugger as the Debug tool, and select the [Initialization File] file:

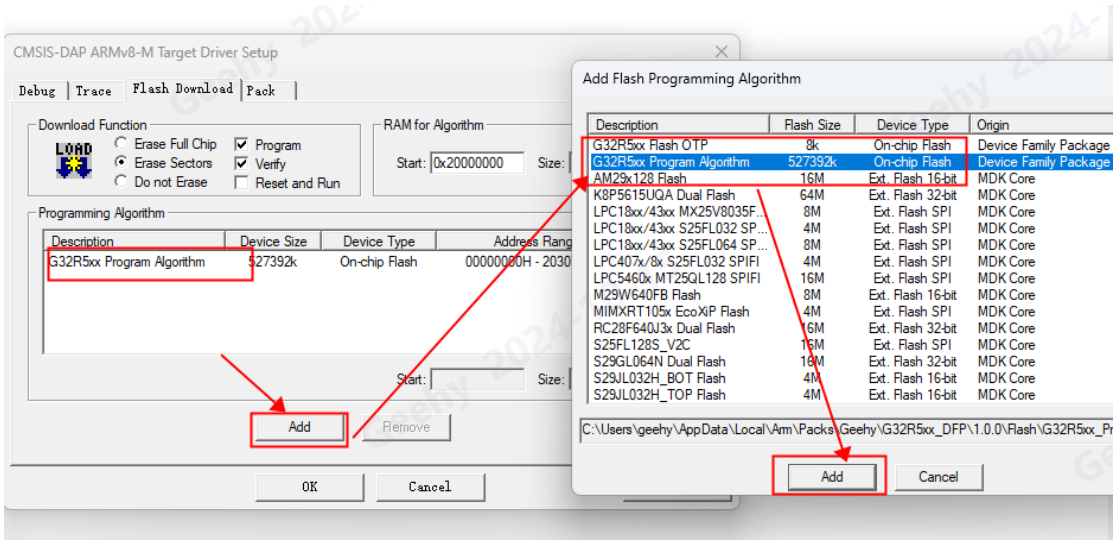




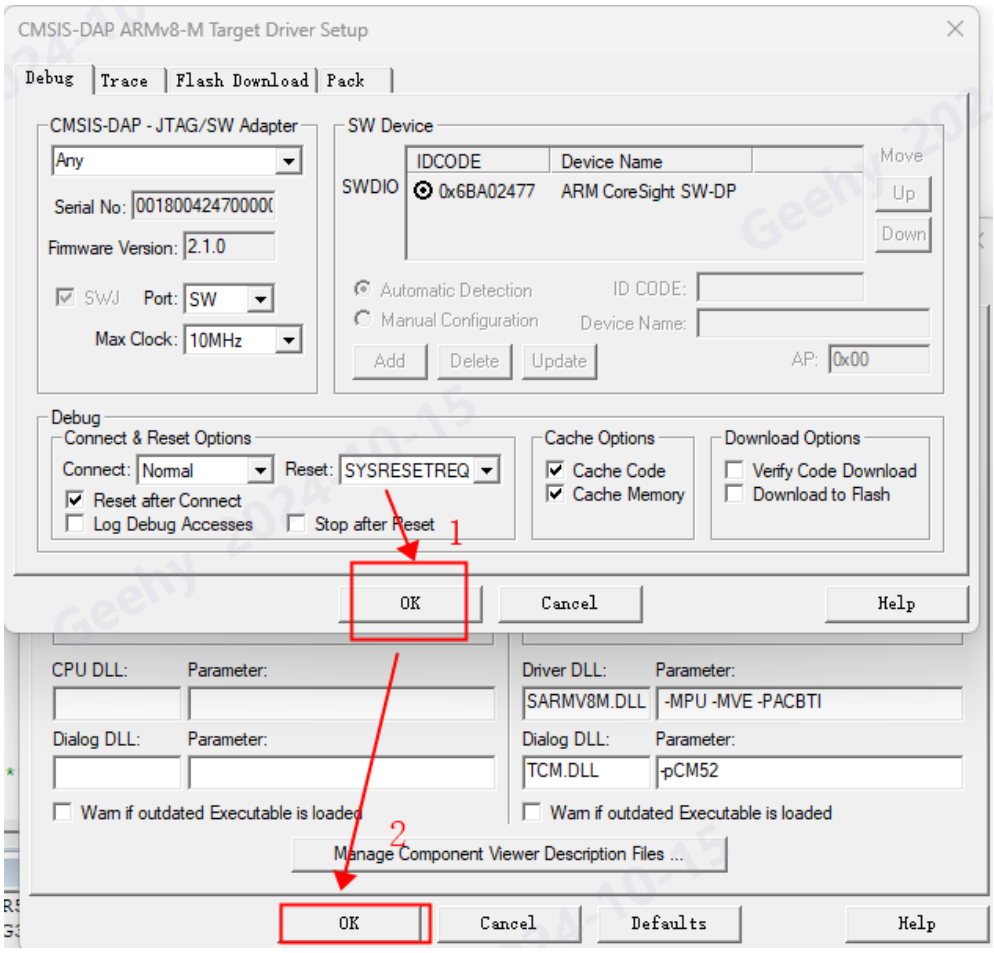
(9) 8. Configure in the Option for Target interface, select the Debug column, click Settings, check Erase Sectors, Program, Verify, and set the start address and size of RAM for Algorithm:

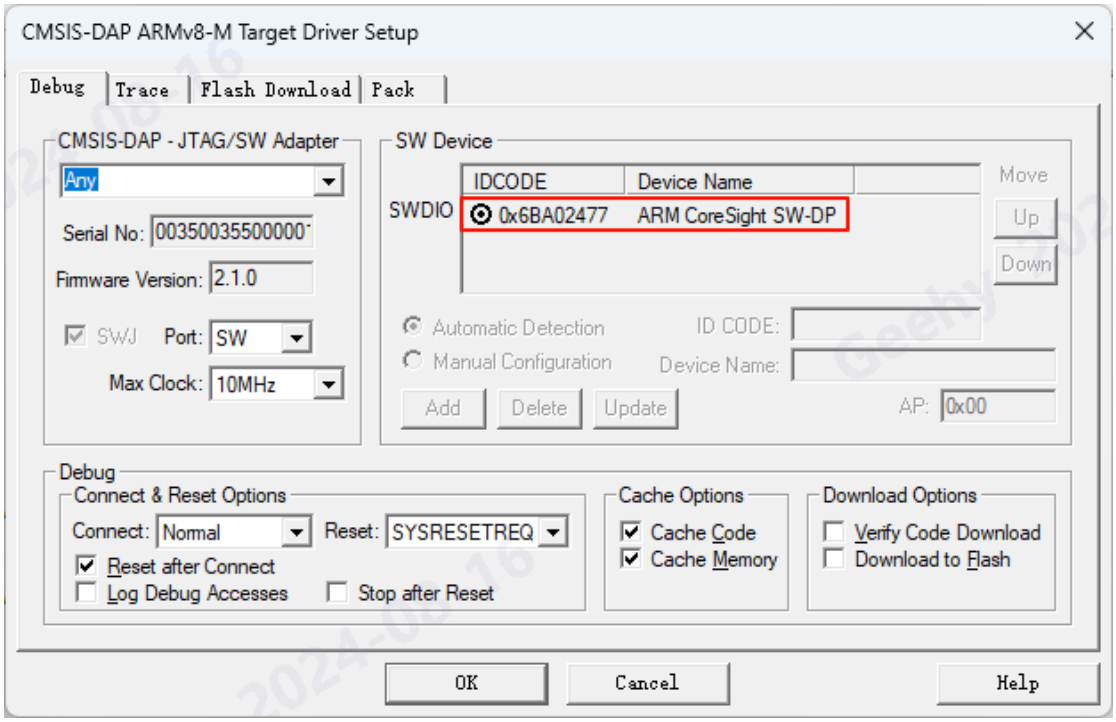


(10) Configure in the Option for Target interface, select the Debug column, click Settings, and select the address and memory size of Program Algorithm:



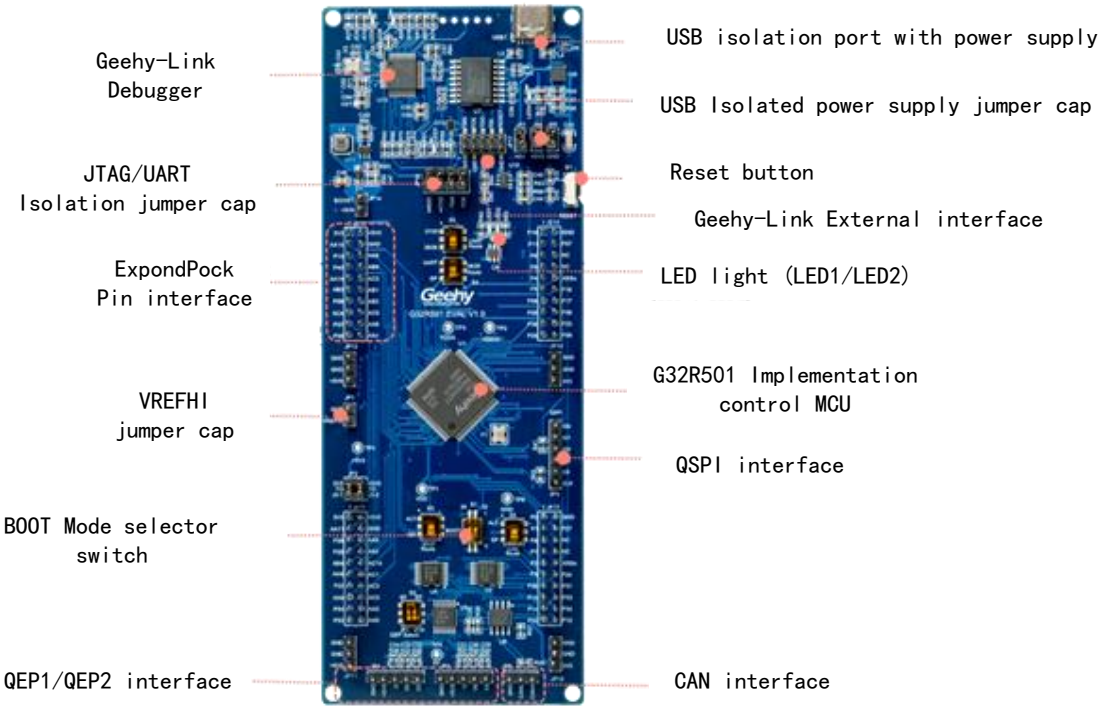
(11) Complete the configuration of Option for Target interface, and before clicking Settings, connect the Evaluation Board to the computer, and the Debug interface should display the IDCODE of debugger correctly:




CMSIS-DAP ARMv8-M Target Driver Setup
Debug
Trace
Flash Download
Pack
CMSIS-DAP - JTAG/SW Adapter
Any
Serial No: 00350035500000
Firmware Version: 2.1.0
SWJ
Port: SW
Max Clock: 10MHz
SW Device
SWDIO
IDCODE
Device Name
0x6BA02477
ARM CoreSight SW-DP
Move
Up
Down
Automatic Detection
Manual Configuration
ID CODE:
Device Name:
Add
Delete
Update
AP: 0x00
Debug
Connect & Reset Options
Connect: Normal
Reset: SYSRESETREQ
Reset after Connect
Log Debug Accesses
Stop after Reset
Cache Options
Cache Code
Cache Memory
Download Options
Verify Code Download
Download to Flash
OK
Cancel
Help

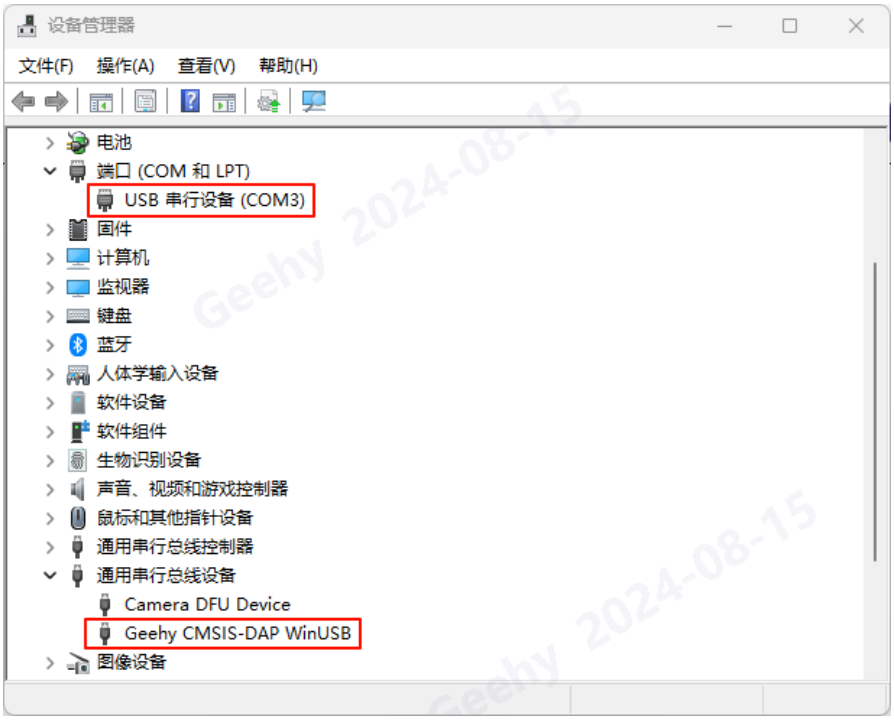
5 Hardware Development Board Wiring

The hardware development board wiring and boot switch selects OFF for S24 and S32.

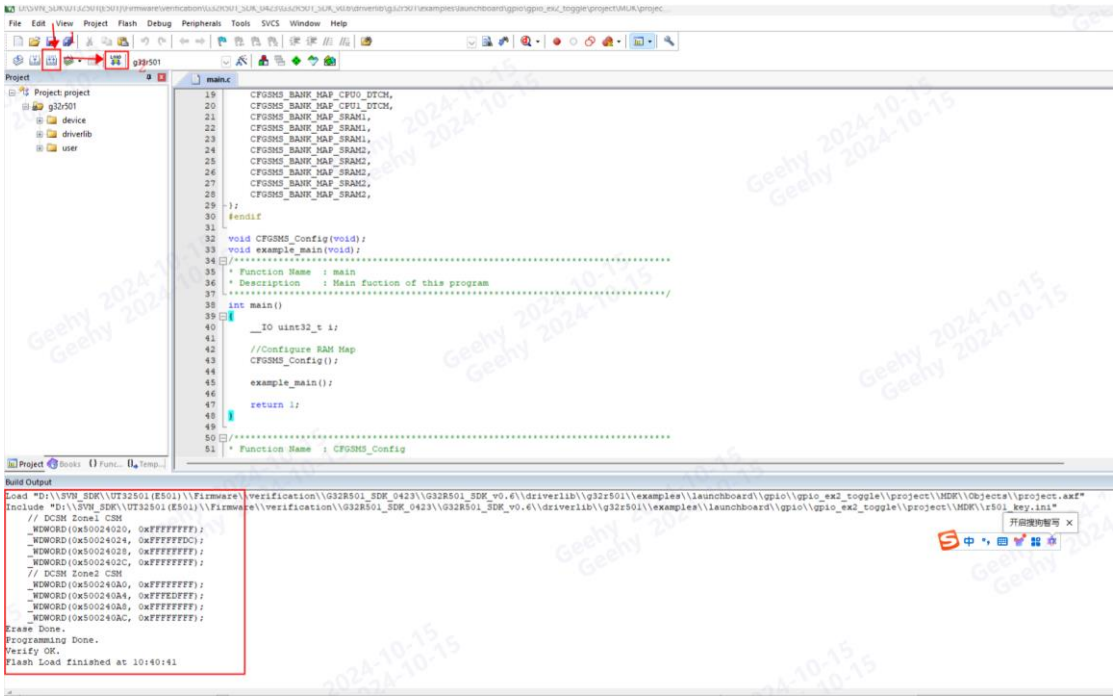


6 Burning Debugging Program

View the status of the debugger drive device

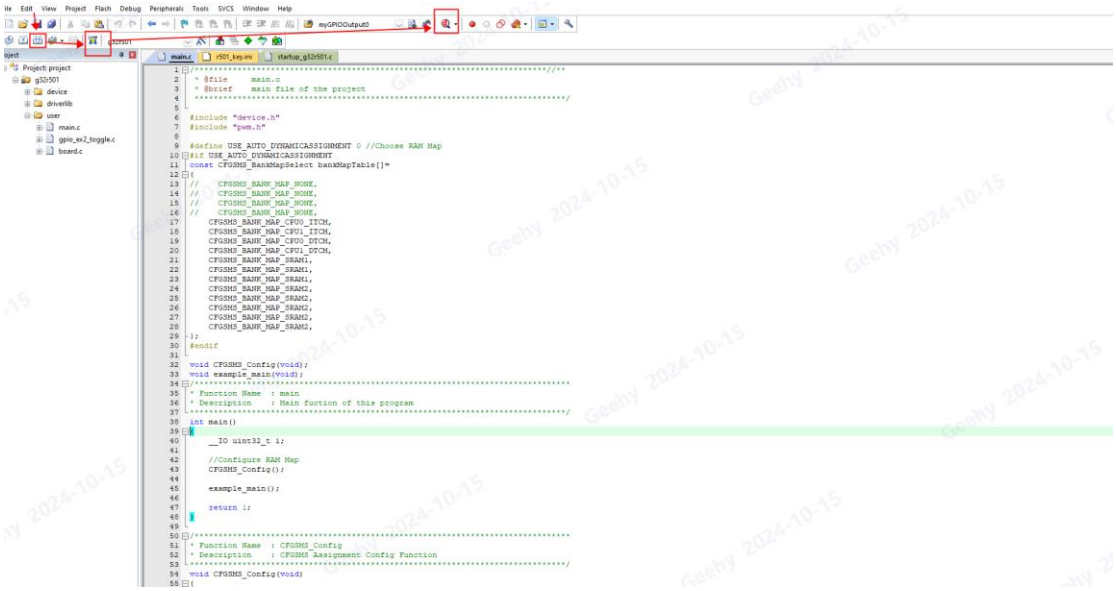


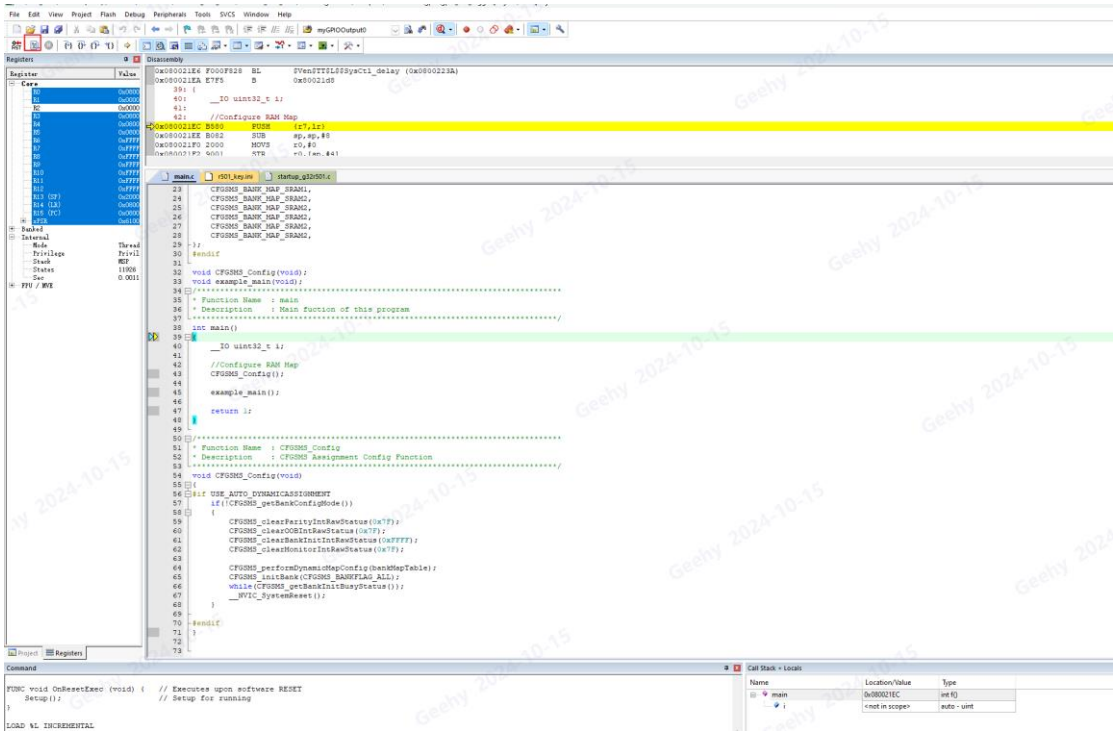
Perform program burning, as shown in the following figure



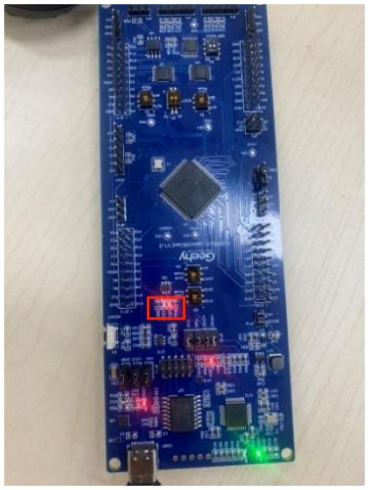
7 Compilation and Download Debugging

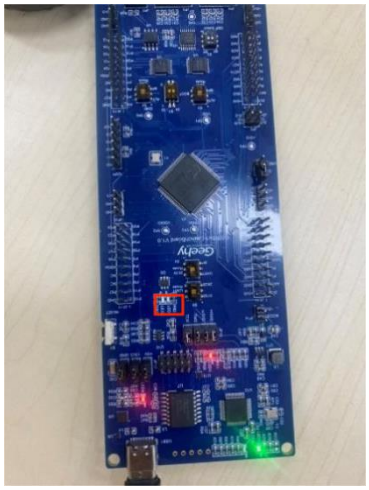
After selecting Build or Rebuild to compile the project, download or start/stop Debug Session debugging as needed.





Running result: The onboard red LED1 flashes, indicating successful running. (LED1 is led out from the GPO23 pin). The phenomenon is shown in the following figure:





8 Common Errors

Note: This section will be updated later.

9 Revision history

Table 4 Document Revision History

Date	Version	Revision History
January, 2025	1.0	New

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